

What is Claimed is:

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1 1. A semiconductor device comprising a source region, a channel
2 region, a drain region, a gate electrode formed on the channel region,
3 and a drift region formed between the channel region and the drain
4 region,
5 wherein the drift region is formed shallowly at least below
6 the gate electrode but formed deeply in a neighborhood of the drain
7 region.

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1 2. A semiconductor device comprising:
2 a first conductivity type well region formed in a first
3 conductivity type semiconductor substrate;
4 a gate electrode formed on the substrate via a gate insulating
5 film;
6 a first conductivity type body region formed to be adjacent
7 to the gate electrode;
8 a second conductivity type source region and a channel region
9 formed in the first conductivity type body region;
10 a second conductivity type drain region formed at a position
11 remote from the first conductivity type body region; and
12 a second conductivity type drift region formed shallowly from
13 the channel region to the drain region, at least below the gate
14 electrode, and formed deeply in a neighborhood of the drain region.

1 3. A semiconductor device according to claim 2, wherein the
2 second conductivity type drift region is formed by implanting at
3 least two kind second conductivity type impurities which have

4 different diffusion coefficients and at least one kind first
5 conductivity type impurity which has a diffusion coefficient
6 substantially equal to or larger than the diffusion coefficient of
7 at least one kind second conductivity type impurity such that it
8 is formed by diffusing the second conductivity type impurities into
9 a deep region by using a difference in the diffusion coefficients
10 and is formed shallowly in a neighborhood of the source region by
11 canceling the second conductivity type impurities by the first
12 conductivity type impurity.

1 4. A semiconductor device according to claim 3, wherein the
2 second conductivity type drift region is formed by implanting an
3 arsenic ion and a phosphorus ion as the second conductivity type
4 impurities into an overall surface of a region serving as the drift
5 region and selectively implanting a boron ion as the first
6 conductivity type impurity only into a region in a neighborhood of
7 the source region.

1 5. A method of manufacturing a semiconductor device including
2 a first conductivity type well region formed in a first conductivity
3 type semiconductor substrate, a gate electrode formed on the
4 substrate via a gate insulating film, a first conductivity type body
5 region formed to be adjacent to the gate electrode, a second
6 conductivity type source region and a channel region formed in the
7 first conductivity type body region, a second conductivity type
8 drain region formed at a position remote from the first conductivity
9 type body region, and a second conductivity type drift region formed
10 shallowly from the channel region to the drain region, at least below

11 the gate electrode, and formed deeply in a neighborhood of the drain
12 region,

13 wherein the steps of forming the drift region, comprising
14 the steps of:

15 implanting two kind second conductivity type impurities to
16 form a second conductivity type low concentration layer
17 constituting the drift region in the first conductivity type well
18 region in the first conductivity type semiconductor substrate via
19 postprocessing;

20 implanting selectively the first conductivity type impurity
21 into a region located in a neighborhood of the source region; and
22 diffusing impurities under a condition that a diffusion
23 coefficient of the first conductivity type impurity is set equal
24 to or larger than a larger one of diffusion coefficients of the second
25 conductivity type impurities.

1 6. A method of manufacturing a semiconductor device,
2 comprising the steps of:

3 ion-implanting two kind second conductivity type impurities
4 to form a second conductivity type low concentration layer serving
5 as a drift region in a first conductivity type well region in a first
6 conductivity type semiconductor substrate via postprocessing;

7 forming a LOCOS oxide film by oxidizing selectively a certain
8 region on the substrate, and forming the second conductivity type
9 low concentration layer at a relatively deep position in the first
10 conductivity type well region and on a surface layer of the substrate
11 by using a difference in diffusion coefficients of two kind second
12 conductivity type impurities respectively;

13 ion-implanting and diffusing a first conductivity type
14 impurity into the surface layer of the substrate of a source forming
15 region via a mask which is formed on a drain forming region on the
16 substrate so as to cancel the second conductivity type layer formed
17 at the relatively deep position in the first conductivity type well
18 region of the source forming region by a diffusion of the first
19 conductivity type impurity;

20 forming a gate insulating film on the substrate, then forming
21 a gate electrode to extend from the gate insulating film to the LOCOS
22 oxide film, and then forming a first conductivity type body region
23 adjacently to one end portion of the gate electrode by implanting
24 and diffusing the first conductivity type impurity via a mask which
25 is formed to cover the gate electrode and the drain forming region;
26 and

27 forming a source/drain region by implanting the second
28 conductivity type impurities via a mask having opening portions
29 which are located over the source forming region and the drain
30 forming region being formed in the first conductivity type body
31 region.

1 7. A method of manufacturing a semiconductor device,
2 according to claim 6, wherein the second conductivity type low
3 concentration layer serving as the drift region is formed by
4 implanting two kind second conductivity type impurities which have
5 different diffusion coefficients and the first conductivity type
6 impurity which has a diffusion coefficient substantially equal to
7 or larger than the diffusion coefficient of one kind second
8 conductivity type impurity of two kind second conductivity type

9 impurities such that it is formed by diffusing the second
10 conductivity type impurities into a deep region by using a
11 difference in the diffusion coefficients and also formed shallowly
12 in a neighborhood of the source region by canceling the second
13 conductivity type impurities by the first conductivity type
14 impurity.

1 8. A semiconductor device comprising a first MOS transistor
2 having a source region, a channel region, a drain region, a gate
3 electrode formed on the channel region, and a drift region formed
4 between the channel region and the drain region, and a second MOS
5 transistor having a source region, a channel region, a drain region,
and a gate electrode formed on the channel region,

6 wherein the drift region of the first MOS transistor is
7 formed shallowly at least below the gate electrode but formed deeply
8 in a neighborhood of the drain region and
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10 a source/drain region of the second MOS transistor consists
11 of a low concentration source-drain region, a high concentration
12 source-drain region, and a middle concentration source/drain region
13 whose concentration is higher than that of the low concentration
14 source/drain region but lower than that of the high concentration
15 source/drain region.

1 9. A semiconductor device comprising a first MOS transistor
2 and a second MOS transistor formed on a first conductivity type
3 semiconductor substrate;

4 wherein the first MOS transistor includes,

5 a first conductivity type well region formed in the

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semiconductor substrate,

a first gate electrode formed on the first conductivity type well region via a first gate insulating film,

a first conductivity type body region formed to be adjacent to the first gate electrode,

a second conductivity type source region and a channel region formed in the first conductivity type body region,

a second conductivity type drain region formed at a position remote from the first conductivity type body region, and

a second conductivity type drift region formed shallowly from the channel region to the drain region, at least below the gate electrode, and formed deeply in a neighborhood of the drain region, and

wherein the second MOS transistor includes,

a second conductivity type well region formed in the semiconductor substrate,

a second gate electrode formed on the second conductivity type well region via a second gate insulating film, and

a source/drain region consisting of a low concentration source/drain region formed to be adjacent to the second gate electrode, a high concentration source/drain region, and a middle concentration source/drain region whose concentration is higher than that of the low concentration source/drain region but lower than that of the high concentration source/drain region.

10. A semiconductor device according to claim 9, wherein the first MOS transistor consists of an N-channel LDMOS transistor, and

3 the second MOS transistor consists of a P-channel high breakdown
4 voltage MOS transistor.

1 11. A method of manufacturing a semiconductor device which
2 includes a first MOS transistor having a body region in which a source
3 region and a channel region are formed, a drain region separated
4 from the body region, a gate electrode formed on the channel region,
5 and a drift region formed between the channel region and the drain
6 region, and a second MOS transistor having a source region, a channel
7 region, a drain region, and a gate electrode formed on the channel
8 region,

9 steps of forming a source/drain region of the second MOS
10 transistor comprising at least a same step as the step of forming
11 the body region of the first MOS transistor.

1 12. A method of manufacturing a semiconductor device,
2 according to claim 11, wherein the step of forming the source/drain
3 region of the second MOS transistor has at least a same step as the
4 step of forming the drift region.

1 13. A method of manufacturing a semiconductor device
2 according to claim 11, in which a first MOS transistor and a second
3 MOS transistor are formed on a first conductivity type semiconductor
4 substrate, comprising the steps of:

5 ion-implanting two kind second conductivity type impurities
6 having a different diffusion coefficient via a mask which has an
7 opening portion over a part of a first conductivity type well region
8 on a first conductivity type semiconductor substrate on which the

9 first conductivity type well region and a second conductivity type
10 well region are formed;

11 forming an oxidation resisting film in a certain region on
12 the substrate, then forming a LOCOS oxide film by oxidizing
13 selectively the substrate while using the oxidation resisting film
14 as a mask, and forming second conductivity type low concentration
15 layers at a relatively deep position in the first conductivity type
16 well region and on a surface layer of the substrate by using a
17 difference in diffusion coefficients of two kind second
18 conductivity type impurities respectively;

19 ion-implanting and diffusing a first conductivity type
20 impurity into a source forming region in the first conductivity type
21 well region and the surface layer of the substrate in a source/drain
22 forming region in the second conductivity type well region via a
23 mask, which has opening portions over the source forming region in
24 the first conductivity type well region and the source/drain forming
25 region in the second conductivity type well region, so as to cancel
26 the second conductivity type layer formed at the relatively deep
27 position in the source forming region in the first conductivity type
28 well region by a diffusion of the first conductivity type impurity
29 and to form a first conductivity type source/drain region in the
30 source/drain forming region in the second conductivity type well
31 region;

32 forming a first gate insulating film in a region other than
33 the LOCOS oxide film on the first conductivity type well region,
34 and forming a second gate insulating film in a region other than
35 the LOCOS oxide film on the second conductivity type well region;

36 forming a first gate electrode and a second gate electrode

37 on the first gate insulating film and the second gate insulating
38 film respectively;

39 ion-implanting and diffusing the first conductivity type
40 impurity via a mask, which covers the first gate electrode in the
41 first conductivity type well region and the drain forming region
42 and has an opening portion over a part of the source/drain forming
43 region on the second conductivity type well region, so as to form
44 a first conductivity type body region adjacently to one end portion
45 of the first gate electrode and to form a second first conductivity
46 type source/drain region in a region separated from the second gate
47 electrode;

48 forming a first second conductivity type source region by
49 implanting the second conductivity type impurities via a mask having
50 an opening portion located over the source forming region in the
51 first conductivity type well region;

52 forming sidewall spacer films on side wall portions of the
53 first gate electrode and the second gate electrode, and then forming
54 a second first conductivity type source/drain region by implanting
55 the first conductivity type impurity via a mask having an opening
56 portion located over the source/drain forming region in the first
57 conductivity type well region; and

58 forming a third first conductivity type source/drain region
59 by implanting the first conductivity type impurity via a mask having
60 at least an opening portion, which is smaller than the second first
61 conductivity type source/drain region, located over the second
62 conductivity type well region.

1 14. A method of manufacturing a semiconductor device

2 according to claim 13, wherein the second conductivity type low
3 concentration layer is formed by utilizing a difference in diffusion
4 coefficients between two type second conductivity type impurities
5 having a different diffusion coefficient and the first conductivity
6 impurity having a diffusion coefficient which is almost equal to
7 or larger than a diffusion coefficient of one of the second
8 conductivity type impurities.

1 15. A method of manufacturing a semiconductor device
2 according to claim 13, wherein concentration of the second first
3 conductivity type source/drain region is set to a middle
4 concentration which is higher than a concentration of the first
5 conductivity type source/drain region but lower than a
6 concentration of the third first conductivity type source/drain
7 region.

1 16. A method of manufacturing a semiconductor device
2 according to claim 11, wherein the first MOS transistor consists
3 of an N-channel LDMOS transistor, and the second MOS transistor
4 consists of a P-channel high breakdown voltage MOS transistor.

1 17. A semiconductor device according to claim 1, wherein the
2 semiconductor device is arranged in plural via a element isolation
3 film, and
4 a channel stopper layer is formed under the element isolation
5 film.

1 18. A method of manufacturing a semiconductor device

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Fig. 2

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2 according to claim 6, further comprising the steps of:

3 ion-implanting two kind second conductivity type impurities
4 to form the second conductivity type low concentration layer serving
5 as the drift region in the first conductivity type well region in
6 the first conductivity type semiconductor substrate via
7 postprocessing;

8 forming an oxidation resisting film on the substrate, and
9 then ion-implanting the first conductivity type impurity into a
10 surface of the substrate via a mask which is formed to cover the
11 oxidation resisting film;

12 forming a first LOCOS oxide film and a second LOCOS oxide
13 film by oxidizing selectively certain regions on the substrate while
14 using the oxidation resisting film as a mask, and forming the second
15 conductivity type low concentration layer at a relatively deep
16 position in the first conductivity type well region and on a surface
17 layer of the substrate respectively by using a difference in
18 diffusion coefficients of two kind second conductivity type
19 impurities, and then forming a channel stopper layer under the
20 second LOCOS oxide film;

21 ion-implanting and diffusing the first conductivity type
22 impurity into the surface layer of the substrate in the source
23 forming region via a mask which is formed in the drain forming region
24 on the substrate so as to cancel the second conductivity type layer
25 formed at the relatively deep position in the first conductivity
26 type well region in the source forming region by the diffusion of
27 the first conductivity type impurity;

28 forming the gate insulating film in a region other than the
29 first LOCOS oxide film and the second LOCOS oxide film on the

30 substrate, then forming the gate electrode to extend from the gate
31 insulating film to the first LOCOS oxide film, and then forming the
32 first conductivity type body region adjacently to one end portion
33 of the gate electrode by implanting and diffusing the first
34 conductivity type impurity via a mask which is formed to cover the
35 gate electrode and the drain forming region; and
36 forming the source/drain region by implanting the second
37 conductivity type impurities via a mask having opening portions
38 which are located over the source forming region and the drain
39 forming region formed in the first conductivity type body region.

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